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PATENT

Test Compaction Using Linear-Matrix Driven Scan Chains

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CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application Number 60/473,380, filed May 23, 2003.

FIELD OF THE INVENTION

[0002] The invention is related to the field of testing integrated circuits.

BACKGROUND OF THE INVENTION

[0003] Design for Testability (DFT) is an important requirement for today's complex application specific integrated circuit (ASIC) designs. DFT techniques allow one to perform high quality manufacturing tests after a chip has been synthesized, and to sort out good chips from bad ones. However, due to the ever increasing complexity of today's designs, the Automatic Test Equipment (ATE) tools required for testing are quite complex and expensive. As a result, manufacturing test costs have become a major part of the overall manufacturing cost of ASICs. Conventional testing approaches are unable to reduce this cost without sacrificing the test quality.

[0004] For example, the use of scan based Automatic Test Pattern Generation (ATPG) is a common DFT methodology that is widely used. Scan logic allows an internal sequential element of an ASIC, such as a flip-flop, to be controlled and observed during testing. The flip-flops are connected into several chains, called scan chains, which are usually accessed through test pins, as shown in **Figure 1**. The test pins are normally shared with the functional chip pins. When testing is performed, the test vector data is

applied through the chains to control the sequential state of the circuit to a desired state. After application of a test vector, the test response data is captured by the flip-flops. The response data is shifted out through the scan chains and is compared against the expected response to check if the chip is functioning correctly.

[0005] To achieve a high quality of the test, it is important to include most, if not all, of the flip-flops in the chip in the scan chains. The number of scan chains is usually limited to 16 or 32. The limit on the number of scan chains is bounded by the number of available input and output (I/O) pins that are able to access the chains, and by the number of scan-channels on an ATE used to drive the chains. Normally, one input and one output pin is required to access each chain. The chains are usually balanced as much as possible to minimize the length of the longest chain. The number of tester cycles required to shift data through a chain is determined by the length of the chain, i.e. by the number of flip-flops in the chain. Therefore, the length of the chains is limited to the number of pins, and the reduction in testing time is limited by the length of the chains. This conventional approach is inadequate for testing integrated circuits, because the required amount of testing time is inefficient for testing modern circuit designs.

[0006] Increasing the number of scan chains would reduce the maximum length of a scan chain, thus reducing the number of test cycles required to shift data through the chains. This directly impacts the test cost by reducing the test application time, but has no affect on the test data required to be stored in tester memory. However, conventional approaches fail to efficiently and cost-effectively do this.

[0007] For example, on-chip pseudo-random test generators based on Linear Feedback Shift Register (LFSR) or some derivation of it, are classified as Logic BIST

techniques which are able to generate test vectors on chip. Hence, they can drive many more parallel scan chains. The data at the output of the chains is fed into an on-chip logic which computes a signature for the output response. This signature is finally serially shifted out to check the test response, or compared against the expected value stored on chip. For a given number of vectors, it would allow one to reduce the test application time, as well as test data required to be stored in tester memory. However, due to the randomness of the generated test patterns, the test quality is degraded. Such techniques are not able to achieve test results having a sufficient level of fault coverage for random logic designs.

[0008] Another method uses a hybrid approach of an LFSR based on-chip test generator, and an external scan based ATPG [1-7] tool. This uses the on-chip LFSR based test generator to drive several parallel scan chains. The ATPG tool is used to target test vectors that can be generated through the LFSR. Additional methods based on this hybrid approach add flexibility to the testing by several different techniques to allow generation of suitable test vectors, such as changing the state of the LFSR (also known as reseeding the LFSR), reconfiguring the LFSR by controlling the feedback taps on the LFSR, or by adding a phase-shifter at the output of the LFSR to change certain outputs of the LFSR as desired.

[0009] However, the hybrid techniques are inefficient, because designing the on-chip test generator, and modifying conventional ATPG tools to derive necessary seeds and/or feedback taps, are both expensive processes.

SUMMARY OF THE INVENTION

[0010] A method of test compaction using linear matrix driven scan chains includes dividing pins of an integrated circuit into a first group and a second group, logically associating each pin of the first group to each pin of the second group, and generating a scan chain in the integrated circuit for each logical association of pins.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **Figure 1** shows a conventional scan design uses available scan pins to drive scan chains, where each chain requires one scan-in and one scan out pin.

[0012] **Figure 2** shows an example of a linear matrix, driven by scan pins, to drive a large number of internal scan chains.

[0013] **Figure 3** shows another example of a linear matrix, driven by scan pins, to drive a large number of internal scan chains.

[0014] **Figure 4** shows an example of a method of performing linear matrix based test compaction.

DETAILED DESCRIPTION

[0015] A linear matrix testing technique for an integrated circuit can be used to drive many parallel scan chains with a handful of chip pins, and can use a scan-based automatic test pattern generator (ATPG) tool to generate high quality test vectors. The linear matrix based methodology compacts the testing of application specific integrated circuit (ASIC) designs. For example, when compared to conventional scan methods, the linear matrix based approach reduces the test application time as well as the required tester memory and test data by an order of magnitude or greater without deteriorating the test quality.

[0016] To provide this test compaction, a linear matrix is used to drive a large number of parallel scan chains from a small set of chip pins. A multiple input shift register (MISR) may be used at the end of each chain to receive and compress the output response of scan chains By increasing the number of parallel scan chains, the size of the longest scan chain is reduced which directly impacts the number of test cycles required to shift data through the chains. This allows the test application time required for shifting data through scan chains to be considerably reduced, by a factor of 10 to 50 or more, depending upon the size of the design and available pins for test. It also reduces the test data required to be stored in the ATPG tester's memory. This considerably reduces the manufacturing test cost, and allows the reuse of older generation testers, which have smaller memories than newer testing tools, and are therefore less expensive. This technique can also be applied to reduced-tester-pin-count-testing, which is an attractive approach to test bare dies before it is packaged.

Linear-Matrix Driven Scan Chain Design

[0017] The test compaction technique uses a linear matrix, driven by scan pins (which can be shared with functional pins), to drive a large number of internal scan chains, as shown in **Figure 2**. The linear matrix is obtained by first dividing the available test pins into two groups, ***Group A*** and ***Group B***. Scan chains are driven by *ExORing* the scan pins from these two groups. Let *Group A* contain ***"n"*** pins, and *Group B* contain ***"m"*** pins. These pins can be used to drive ***n*m*** chains as follows:

Let the pins in ***Group A*** be represented as ***SIa[i], i: 1*** to ***n***

Let the pins in ***Group B*** be represented as ***SIb[j], j: 1*** to ***m***

Let the scan-in of ***(n*m)*** chains be represented as ***C[i][j], i: 1*** to ***n***, ***j: 1*** to ***m***;

Each ***C[i][j]*** is obtained by performing ***ExOR*** on input ***SIa[i]*** and ***SIb[j]***, i.e.

C[i][j] <= SIa[i] ExOR SIb[j], i ranges from 1 to ***n, j ranges from 1*** to ***m. (1)***

[0018] The number of chains driven by the matrix can be controlled by the distribution of the available scan pins in the two groups (Group A and Group B). To get a maximum number of scan chains, the pins may be divided equally between the two groups, i.e. for optimal results, either $n = m$, or $n = m+1$. Therefore, as shown in **Figure 2**, the linear matrix driven ***(n*m)*** scan chains, gives 9 chains from 6 pins

[0019] Using a linear *ExOR* matrix to drive internal scan chains may affect the independence of the individual bits being scanned into these chains at a given instant. However, due to the fact that for any given fault in a design, only a few scan bits may need to be set to specific values, there may be practically little to no degradation in the test quality. An ATPG program is used to generate a test vector that determines the scan

inputs for each chain C[i][j]. Equation 1 above is used to determine the values for SIa[i] and SIb[j] which, when applied to an *ExOR* operation, cause the generated test vector values to be applied to the input of the scan chain C[i][j]. Unspecified bits may be filled with random values.

[0020] The number of internal chains can be further increased by directly driving additional ***n*** chains from ***Group A*** scan pins, as shown in **Figure 3**, without further limiting the independence of bits being scanned, as follows:

C[i][j] <= SIa[i] ExOR SIb[j], i ranges from ***1*** to ***n, j*** ranges from ***1*** to ***m.***

C[i][j] <= SIa[i], i ranges from ***1*** to ***n, j = m+1*** *giving a total of* ***n*** *** (m+1)*** *chains.* ***(2a)***

Alternatively, this can be represented as

C[i][j] <= SIa[i] ExOR SIb[j], i ranges from ***1*** to ***n, j*** ranges from ***1*** to ***m+1, with SIb[m+1] = 0. (2b)***

[0021] SIb[m+1] may be assumed to be 0, because, if for some vector C[i][j]], SIb[m+1] is set to 1, the same solution C[i][j] may be obtained by inverting each of SIa[i] and SIb[j], thus resetting SIb[m+1] to 0. Since both SIa[i] and SIb[j] are inverted, their *ExOR* result C[i][j] remains unchanged. Since SIb[m+1] is assumed to 0, no external test pin is required to drive this signal.

[0022] A trade off in the number of scan chains, and the relative dependence between the bits being scanned may be made by changing the distribution of pins in ***Group A*** and

Group B. Choosing $m = 0$ reduces the design to conventional scan designs driving the minimal number of chains. The optimal number of scan chains may be achieved when $n = m$ or $n = m+1$. However, there may be practically little or no degradation in test quality or increase in test vectors, as there is sufficient independence in the vectors that can be driven by the linear matrix.

[0023] Output data at internal scan-out pins of each chain is shifted into a multi-input shift register (MISR) of appropriate length. The final state of the MISR that represents the signature of the test response, is either serially shifted out, or is compared with the expected golden signature stored on chip.

[0024] The increase in the number of chains, the reduction in chain length, the reduction in the number of shift cycles, and the reduction in the amount of tester memory, when using the Test Compaction approach, is shown in **Table 1**, where F is the number of flip-flops in a design; P is the number of pins available to access chains; and V is the number of vectors.

Table 1

	Conventional Scan	Linear Matrix Scan
Number of chains	k	$k * (k+1)$ where $k = P/2$
Maximum chain length	F/k	$F/(k*(k+1))$
Number of shift cycles	$V*F/k$	$V * (F/(k*(k+1)) +1)$
Tester scan memory	$2*V*F$	$2*V*(F/(k+1)) + L$

[0025] Thus, both the tester data, as well as the number of tester cycles used to perform the test is reduced by a factor of k. **Table 2** shows an example of the reduction in

manufacturing costs when using the test compaction approach. Assuming ***F** = 40,000;* ***P** = 40;* ***V** = 10,000,* and *test time costs 10¢/sec*, then:

Table 2

	Conventional Scan	*Linear Matrix Scan*	*Advantage Factor*
Number of chains	*20*	*400*	*20*
Maximum chain length	*2000*	*100*	*20*
Number of cycles	*20 Million*	*1 Million*	*20*
Tester scan memory	*800 Mb*	*40 Mb*	*20*
Test time (10 MHz)	*2 sec*	*0.1 sec*	*20*
Test cost for 1M chips (Assuming)	*$2M*	*$100 K*	*20*

[0026] The linear matrix based scheme can therefore significantly reduce the amount of tester memory and the amount of test time, thus reducing the overall manufacturing test cost.

Multidimensional Extension

[0027] The linear matrix based approach can be extended to a linear matrix having more than two dimensions by dividing the pins into more than two groups, and driving the scan chains with an *ExOR* matrix that is connected to a pin from each group. For example, if the available pins are divided into three groups, A, B and C, such that SIa[i] represents pins in Group A, SIb[j] represents pins in group B, and SIc[k] represents pins in group C, then the inputs to a chain can be represented as C[i][j][k]:

C[i][j][k] <= SIa[i] ExOR SIb[j] ExOR SIc[k]. (3)

[0028] This allows (P/3)*(P/3)*(P/3) chains to be driven from P pins. In general, dividing the pins into n groups having an approximately equal number of pins, and using an n-dimensional linear matrix, allows (P/n)*(P/n) ... (P/n) chains to be driven. In other words, the number of chains is equal to (P/n)^n, i.e. (P/n) raised to the power of n, where P is the total number of pins on the chip, and n is the number of groups of pins.

[0029] **Figure 4** shows an example of a method of performing linear matrix based test compaction. Pins of an integrated circuit are divided into multiple groups, 410. For each group, each pin of the group is logically associated with each pin of the other groups by the linear matrix, 420. A scan chain is generated in the integrated circuit for each logical association of pins, 430. The input pins of the integrated circuit to be tested receive signals from a test pattern generator, 440. The signals pass through the linear matrix, 450. For each logical association of pins, the matrix performs a logical operation on the corresponding test signals received by the pins, 460. The results of the logical operations represent the input test vector that is output by the matrix to drive the scan chains during the testing of the integrated circuit, 470.

Testability of the Linear Matrix

[0030] The linear matrix that drives the scan chains is itself easy to test. It is directly controllable from chip pins, and is observable through the scan chains that it feeds. In fact **Table 3** shows the combinations of input vectors at ***Group A*** and ***Group B*** pins that would test the entire linear matrix for single stuck-at faults.

Table 3

Group A (SIa[i] pins)	***Group B (SIb[j] pins)***
1	*0*
1	*1*
0	*1*
0	*0*

[0031] A method of test compaction using linear matrix driven scan chains includes dividing pins of an integrated circuit into a first group and a second group, logically associating each pin of the first group to each pin of the second group, and generating a scan chain in the integrated circuit for each logical association of pins. The linear matrix scheme of test compaction uses an ExOR matrix to drive the chains, using one ExOR gate per chain. It may use a MISR at the scan-chain outputs.

[0032] The test compaction technique can be used to perform reduced-test-pin-count testing. The linear matrix based approach to test compaction reduces the number of cycles required to shift scan data through the chains. It reduces the required number of scan data bits to be stored on an ATE. It retains high fault coverage as opposed to Logic BIST based schemes where the fault coverage is usually not as high for random logic designs. The technique may be performed without an LFSR or on-chip test generator.

[0033] Linear matrix based test compaction may be performed using a combination of hardware logic and computer software programs which are stored in a computer readable medium and executed by a computer processing system. For example, the linear matrix may be implemented as an electronic circuit that receives patterns to be input to

the scan chains from an Automatic Test Pattern Generator, which is implemented as a computer software program stored in a computer readable memory and executed by a computer processing system.

[0034] These and other embodiments of the present invention may be realized in accordance with the above teachings and it should be evident that various modifications and changes may be made to the above described embodiments without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense and the invention measured only in terms of the claims.